ABSTRACT OF THE DISCLOSURE

A method for designing a semiconductor integrated circuit is provided that is capable of a timing simulation that is approximate to an actual operation by reducing the effect of IR drop on the timing without reducing an effective area necessary for arrangement of elements or the number of pads that can be used other than power supply pads and without increasing the processing time. In a FF driving ability change procedure, a flip–flop having a delay time larger than a transition time from a state in which an IR drop occurs in a power supply voltage to a state of an ideal power supply voltage is substituted for an arbitrary flip–flop. Thus, a delay library considering IR drop may be produced previously only for the flop–flop, thus enabling a production time of the library to be reduced and improving the calculation accuracy of the delay time in the delay calculation procedure. Furthermore, the substitution of a flip–flop having a low driving ability enables the area to be reduced.